



Real-Time Signal Filtering on Embedded Systems: A Hardware-Software Co-Design Approach

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Abstract

Real-time digital signal filtering is a fundamental challenge in embedded systems engineering, sitting at the intersection of computer science and electronic engineering. As embedded processors become increasingly powerful while remaining severely resource-constrained, designing efficient filtering algorithms that meet strict timing requirements demands a deep understanding of both hardware architecture and software design.

This paper presents a comprehensive hardware-software co-design approach to implementing real-time digital filters on embedded microcontrollers. We examine three filtering architectures — the Finite Impulse Response (FIR) filter, the Infinite Impulse Response (IIR) filter, and an adaptive Least Mean Squares (LMS) filter — and implement them on an ARM Cortex-M4 microcontroller (STM32F4 series). The system is evaluated on three real-world signals: ECG (electrocardiography) biomedical signals, audio signals, and industrial vibration data from motor sensors.

Our experiments demonstrate that optimized IIR filters achieve a 3.2x speed improvement over naive FIR implementations through strategic use of hardware floating-point units (FPU) and Direct Memory Access (DMA) controllers. The adaptive LMS filter successfully removes 50 Hz power-line interference from ECG signals with an average Signal-to-Noise Ratio (SNR) improvement of 28 dB while consuming only 11 mW of power. These results confirm that careful co-design of algorithms and hardware resources can enable high-quality real-time filtering even on low-cost embedded platforms.

Keywords: Real-time processing; Digital filters; Embedded systems; ARM Cortex-M4; FIR filters; IIR filters; Adaptive filters; Hardware-Software co-design; DSP; Signal-to-Noise Ratio

1. Introduction

Every time a doctor reads an ECG trace, listens to a patient's heartbeat through a digital stethoscope, or analyzes vibration data from an industrial motor, the underlying data has passed through a digital filter. These filters remove unwanted noise, isolate frequency bands of interest, and ensure that the signal a human or algorithm receives is clean and meaningful. Implementing such filters in real time on embedded devices — small, power-constrained microcontrollers without operating systems or powerful processors — is one of the most practically important problems in modern electronic engineering.

The challenge is not merely mathematical. Designing a good filter on paper is a task for signal processing theory. Making it run in real time on a microcontroller that has 168 MHz of processing power, 196 KB of RAM, and a battery budget of a few milliwatts is a hardware-software co-design problem. Every decision — from the choice of filter architecture to the use of hardware peripherals like Direct Memory Access (DMA) and the Floating-Point Unit (FPU) — directly impacts whether the system meets its deadlines.

This paper addresses this challenge by developing, implementing, and evaluating three filter types on an STM32F4 ARM Cortex-M4 microcontroller. We treat the problem from both the computer science



perspective (algorithm design, memory management, real-time scheduling) and the electronic engineering perspective (hardware peripheral configuration, analog-to-digital conversion, power consumption). The goal is to provide a complete, working, and well-explained system that can serve as both a research contribution and a practical reference for engineers working on similar problems.

1.1 Research Objectives

This research aims to:

- Design and implement three digital filter architectures (FIR, IIR, LMS) optimized for embedded constraints.
- Integrate hardware peripherals (DMA, FPU, ADC) to maximize real-time performance.
- Evaluate filter performance on three real-world signal types: biomedical (ECG), audio, and industrial vibration.
- Compare the trade-offs between filter types in terms of computational cost, power consumption, and signal quality.
- Provide a reusable, open hardware-software co-design methodology.

1.2 Paper Organization

Section 2 provides the theoretical background on digital filtering. Section 3 describes the hardware platform and system design. Section 4 presents the software implementation. Section 5 details the experimental setup and results. Section 6 discusses findings and trade-offs, and Section 7 concludes with directions for future work.

2. Theoretical Background

2.1 The Need for Real-Time Filtering

A real-time system is one where correctness depends not only on the logical result of a computation but also on the time at which the result is produced. In signal processing, this means a filter must produce each output sample before the next input sample arrives. For a system sampling at 1 kHz, the filter has exactly 1 millisecond per sample. Missing this deadline — even by a few microseconds — corrupts the output buffer and may cause catastrophic system failure in safety-critical applications like medical devices or industrial controllers.

The embedded constraint adds another layer of difficulty: unlike a desktop computer that can run a fast Fourier transform in milliseconds using SIMD instructions, an embedded microcontroller has no such luxury. The engineer must work with fixed-point or single-precision floating-point arithmetic, limited cache, and carefully managed memory to fit within the processing budget.

2.2 Digital Filter Theory

A digital filter is a discrete-time system that modifies the frequency content of a signal. Given an input sequence $x[n]$, a digital filter produces an output $y[n]$ according to a difference equation. The general form of a linear time-invariant (LTI) causal filter is:

$$y[n] = \sum_{k=0}^{M} b[k] \cdot x[n-k] - \sum_{k=1}^{N} a[k] \cdot y[n-k]$$



Where $b[k]$ are the feedforward (numerator) coefficients, $a[k]$ are the feedback (denominator) coefficients, M is the feedforward order, and N is the feedback order. When all $a[k] = 0$ (no feedback), the filter is an FIR filter. When feedback terms are present, it is an IIR filter.

2.3 Finite Impulse Response (FIR) Filters

An FIR filter of order M computes its output as a weighted sum of the $M+1$ most recent input samples:

$$y[n] = \sum_{k=0}^{M} b[k] \cdot x[n-k]$$

FIR filters are inherently stable (no feedback means no possibility of unstable poles), can achieve perfectly linear phase response, and are straightforward to implement. Their main disadvantage is that achieving sharp frequency selectivity requires a large number of coefficients (high M), which translates directly to computational cost: an order-64 lowpass FIR filter requires 65 multiply-accumulate operations per sample.

In embedded systems, FIR filters are typically implemented using a circular buffer (ring buffer) to efficiently manage the shift register of past input samples, avoiding the $O(M)$ memory copies that a naive implementation would require at each sample.

2.4 Infinite Impulse Response (IIR) Filters

IIR filters use feedback to achieve sharp frequency responses with far fewer coefficients than FIR. A second-order IIR section (called a 'biquad') implements the equation:

$$y[n] = b_0 \cdot x[n] + b_1 \cdot x[n-1] + b_2 \cdot x[n-2] - a_1 \cdot y[n-1] - a_2 \cdot y[n-2]$$

Higher-order IIR filters are implemented as cascaded biquad sections (Direct Form II Transposed structure) to minimize numerical errors. An 8th-order Butterworth lowpass filter requires only 4 biquad sections (20 coefficients and 8 state variables), whereas an equivalent FIR filter might require 128 or more taps. This makes IIR filters highly attractive for resource-constrained embedded systems.

The trade-off is that IIR filters can become unstable if the feedback coefficients are poorly designed, and they always introduce some phase distortion (non-linear phase response). For applications where phase distortion is acceptable — such as audio equalization or industrial vibration monitoring — IIR filters are typically the preferred choice.

2.5 Adaptive Filtering: The LMS Algorithm

Adaptive filters solve a different problem: rather than filtering based on fixed, pre-designed coefficients, they automatically adjust their coefficients in real time to optimize a performance criterion. The Least Mean Squares (LMS) algorithm is the most widely used adaptive filtering algorithm due to its simplicity and computational efficiency.

Given a desired signal $d[n]$ and a reference input $x[n]$, the LMS filter produces an output $y[n] = w^T[n] \cdot x[n]$, where $w[n]$ is the coefficient vector. The error signal is $e[n] = d[n] - y[n]$. The LMS update rule is:

$$w[n+1] = w[n] + 2\mu e[n] \cdot x[n]$$

Where μ (μ) is the step size, a small positive constant that controls the trade-off between convergence speed and steady-state error. In our biomedical application, the reference input $x[n]$ is a 50 Hz sinusoid (the power-line interference), and the desired signal $d[n]$ is the corrupted ECG. The LMS filter learns to subtract exactly the right amount of 50 Hz interference, leaving a clean ECG output.



2.6 ARM Cortex-M4 Architecture and DSP Capabilities

The ARM Cortex-M4 is the most widely deployed processor core for mid-range embedded DSP applications. Key features relevant to real-time filtering include:

- Single-cycle Multiply-Accumulate (MAC) instruction: executes one multiply-add in a single clock cycle, making FIR filter loops extremely efficient.
- Hardware Floating-Point Unit (FPU): IEEE 754 single-precision (32-bit) floating-point operations execute in 1-3 cycles, eliminating the need for slow software floating-point emulation.
- DSP extension instructions: SIMD instructions that process two 16-bit operations in a single 32-bit instruction, doubling throughput for fixed-point algorithms.
- Direct Memory Access (DMA) controller: transfers data between peripherals (ADC, DAC, UART) and memory without CPU involvement, allowing the processor to run filter computations while data transfer happens in parallel.

Understanding and exploiting these hardware features is central to the hardware-software co-design approach presented in this paper.

3. System Hardware Design

3.1 Hardware Platform

The target platform is the STM32F407VG microcontroller mounted on the STM32F4-Discovery development board. This platform was chosen because it represents the state-of-the-art in cost-effective embedded DSP: it offers an ARM Cortex-M4 running at 168 MHz with FPU, 1 MB of Flash, 192 KB of SRAM, a 12-bit ADC, and a 12-bit DAC, all at a cost under \$10. Table 1 summarizes the key hardware specifications.

Table 1. STM32F407VG hardware specifications.

Parameter	Specification	Relevance to Filtering
CPU Core	ARM Cortex-M4 @ 168 MHz	Processing budget per sample
FPU	IEEE 754 Single-Precision	Fast float arithmetic for coefficients
SRAM	192 KB	Filter state + circular buffers
Flash	1 MB	Code + coefficient storage
ADC	12-bit, up to 2.4 MSPS	Signal acquisition
DAC	12-bit, 2 channels	Filtered output
DMA	2 controllers, 16 streams	CPU-free data transfer
Timers	14 timers (up to 168 MHz)	Precise sampling intervals
Supply Voltage	2.0 – 3.6 V	Low-power design
Operating Temperature	-40°C to 85°C	Industrial applicability

3.2 Signal Acquisition Circuit

The signal acquisition front-end consists of the analog signal entering through a BNC connector and passing through a signal conditioning stage made up of a unity-gain buffer amplifier (TL071 op-amp configured as a voltage follower), which provides high input impedance and drives the ADC input without loading the signal source. An RC anti-aliasing filter ($R = 10 \text{ k}\Omega$, $C = 15 \text{ nF}$) with a cutoff frequency of approximately 1.06 kHz prevents aliasing when sampling at 2 kHz. A DC bias network (two 100 k Ω resistors forming a



voltage divider from the 3.3 V supply) centers the signal at 1.65 V to utilize the full ADC range for bipolar signals.

The ADC is configured in continuous scan mode triggered by Timer 2, which generates a precise interrupt at the configured sampling frequency. The ADC result register is read by DMA Stream 0, which automatically transfers each completed conversion to a double-buffered input array in SRAM without any CPU intervention.

3.3 DMA Double-Buffering Architecture

The core data flow architecture uses DMA double buffering (also called ping-pong buffering). Two equal-sized buffers (Buffer A and Buffer B) are alternately filled by the DMA controller. While the DMA writes new samples into Buffer A, the CPU processes the samples already collected in Buffer B. When the DMA completes filling Buffer A (signaled by a DMA transfer-complete interrupt), the roles swap: the DMA begins filling Buffer B while the CPU processes Buffer A.

This architecture ensures that the CPU's filter computation never competes with data acquisition for memory access. The buffer size is chosen to match the processing latency budget: with a 1 kHz sampling rate and 64 samples per buffer, the CPU has 64 ms to process each buffer. At 168 MHz, even the most complex filter we implement completes well within this budget.

3.4 Output Stage

The filtered signal is output through the STM32F407's 12-bit DAC, also driven by DMA. The analog output is buffered by a second TL071 voltage follower stage, then passes through a passive reconstruction filter ($R = 10\text{ k}\Omega$, $C = 47\text{ nF}$, cutoff $\approx 339\text{ Hz}$) before reaching the output BNC connector. An LED indicator on GPIO PA5 toggles with each processed buffer as a visual real-time indicator and allows oscilloscope measurement of the total processing latency.

4. Software Implementation

4.1 Software Architecture Overview

The firmware is written in C99 using the STM32 HAL (Hardware Abstraction Layer) library version 1.28. The build system uses GNU ARM Embedded Toolchain (gcc-arm-none-eabi 12.2). The software architecture follows a layered design: the Hardware Layer handles ADC/DAC/DMA/Timer configuration; the Signal Layer provides the three filter implementations; and the Application Layer orchestrates the processing pipeline.

All filtering is performed in single-precision floating-point (float32_t from CMSIS-DSP). The FPU is enabled in the system startup code by setting FPCCR and CPACR registers. The CMSIS-DSP library provides optimized ARM assembly implementations of the core filter routines, which we use for benchmarking comparison.

4.2 FIR Filter Implementation

The FIR filter uses a circular buffer (ring buffer) to maintain the delay line of past input samples. The implementation is shown below:

```
/* FIR Filter Structure */
typedef struct {
    float32_t  coeffs[FIR_ORDER + 1]; /* Filter coefficients (const) */
    float32_t  state[FIR_ORDER + 1];  /* Delay line circular buffer */
}
```



```

uint16_t  index;                /* Current write position */
uint16_t  order;               /* Filter order M */
} FIR_Filter_t;

/* Process one sample - optimized with MAC instruction */
__attribute__((optimize("O3")))
float32_t FIR_Process(FIR_Filter_t *f, float32_t input) {
    float32_t acc = 0.0f;
    uint16_t  idx = f->index;
    f->state[idx] = input;
    /* Unrolled MAC loop - compiler generates VLMA.F32 instructions */
    for (uint16_t k = 0; k <= f->order; k++) {
        acc += f->coeffs[k] * f->state[(idx - k) & f->order];
    }
    f->index = (idx + 1) & f->order;
    return acc;
}

```

The coefficients are designed using the Parks-McClellan (Remez exchange) algorithm via MATLAB's `firpm()` function, which produces the optimal equiripple filter for a given specification. For a 64th-order lowpass FIR filter with a 400 Hz passband and 500 Hz stopband at 2 kHz sampling rate, the algorithm achieves 60 dB stopband attenuation.

4.3 IIR Filter Implementation (Cascaded Biquads)

The IIR filter is implemented as cascaded second-order sections (SOS) in Direct Form II Transposed structure, which provides the best numerical stability for fixed-point and single-precision floating-point implementations. Each biquad section maintains two state variables (w_1 and w_2):

```

/* Biquad Section Structure */
typedef struct {
    float32_t b0, b1, b2; /* Numerator coefficients */
    float32_t a1, a2; /* Denominator coefficients */
    float32_t w1, w2; /* State variables (delay) */
} Biquad_t;

/* Process one sample through one biquad section */
static inline float32_t Biquad_Process(Biquad_t *b, float32_t x) {
    float32_t y = b->b0 * x + b->w1;
    b->w1 = b->b1 * x - b->a1 * y + b->w2;
    b->w2 = b->b2 * x - b->a2 * y;
    return y;
}

/* 8th-order Butterworth Lowpass - 4 biquad sections */
float32_t IIR_Process(Biquad_t sections[], uint8_t n, float32_t x) {
    for (uint8_t i = 0; i < n; i++) x = Biquad_Process(&sections[i], x);
    return x;
}

```

The biquad coefficients are generated using `scipy.signal.butter()` in Python and exported as C header files. An 8th-order Butterworth lowpass filter at 400 Hz requires only 4 biquad sections with 5 coefficients each (20 total), compared to 65 coefficients for the equivalent FIR filter.



4.4 Adaptive LMS Filter Implementation

The LMS adaptive filter is implemented for real-time noise cancellation. The reference input (50 Hz sinusoid) is generated internally by the microcontroller's timer, phase-synchronized with the power line frequency using a Phase-Locked Loop (PLL) algorithm:

```
/* LMS Adaptive Filter Structure */
typedef struct {
    float32_t  weights[LMS_ORDER]; /* Adaptive coefficients w[n] */
    float32_t  ref_buf[LMS_ORDER]; /* Reference signal delay line */
    float32_t  mu; /* Step size (convergence rate) */
    uint16_t   order; /* Filter length */
} LMS_Filter_t;

/* LMS Update: cancels noise from d[n] using reference x[n] */
float32_t LMS_Process(LMS_Filter_t *f, float32_t d, float32_t ref) {
    /* Shift reference buffer */
    memmove(&f->ref_buf[1], &f->ref_buf[0],
            (f->order - 1) * sizeof(float32_t));
    f->ref_buf[0] = ref;

    /* Compute filter output y[n] = w^T * x */
    float32_t y = 0.0f;
    for (uint16_t k = 0; k < f->order; k++)
        y += f->weights[k] * f->ref_buf[k];

    /* Error signal: e[n] = d[n] - y[n] */
    float32_t e = d - y;

    /* Weight update: w[n+1] = w[n] + 2*mu*e[n]*x[n] */
    float32_t step = 2.0f * f->mu * e;
    for (uint16_t k = 0; k < f->order; k++)
        f->weights[k] += step * f->ref_buf[k];

    return e; /* Return cleaned signal */
}
```

The step size $\mu = 0.005$ was selected experimentally to balance convergence speed (approximately 200 ms to steady state at 1 kHz) with residual noise floor. A normalized LMS (NLMS) variant, which automatically adjusts μ based on input power, was also implemented and compared.

4.5 Real-Time Scheduling and Interrupt Handling

The system runs without an RTOS. Processing is entirely interrupt-driven: the DMA transfer-complete interrupt sets a global flag, and the main loop polls this flag and dispatches the appropriate filter. This super-loop architecture is sufficient because the system is single-purpose, but Section 6 discusses how an RTOS like FreeRTOS would be beneficial in multi-sensor applications.

Interrupt latency was measured using the Cortex-M4 Data Watchpoint and Trace (DWT) cycle counter. The worst-case interrupt entry latency (from interrupt assertion to first instruction execution) was measured at 12 clock cycles (71 ns at 168 MHz), well within the 1 ms sample period budget.

5. Experimental Results and Evaluation



5.1 Experimental Setup

All experiments were conducted with the STM32F4-Discovery board powered by a bench supply at 3.3 V. Signal input was generated by an Agilent 33220A function generator for synthetic signals, and a PhysioBank MIT-BIH Arrhythmia Database recording for ECG signals (digitized at 360 Hz, upsampled to 1 kHz). Current consumption was measured using a Nordic Semiconductor PPK2 (Power Profiler Kit 2) with 10 μ A resolution. Processing time was measured using the DWT cycle counter with 5.95 ns resolution at 168 MHz. All reported values are averages over 10,000 samples.

5.2 Computational Performance

Table 2 shows the execution time in CPU clock cycles for each filter type, measured processing one 64-sample buffer at 168 MHz.

Table 2. Filter computational performance at 168 MHz.

Filter Type	Cycles/Sample	Time/Sample (μ s)	Time/Buffer (ms)	CPU Load (%)
FIR Order-64 (naive)	412	2.45	0.157	24.5%
FIR Order-64 (CMSIS-DSP)	198	1.18	0.075	11.8%
FIR Order-64 (optimized)	128	0.76	0.049	7.6%
IIR 8th-order Butterworth	87	0.52	0.033	5.2%
LMS Order-32 ($\mu=0.005$)	156	0.93	0.060	9.3%
LMS Order-32 (NLMS)	175	1.04	0.067	10.4%

The optimized IIR filter achieves the lowest computational cost, requiring only 87 cycles per sample compared to 412 for the naive FIR implementation — a 4.7x improvement. This confirms the theoretical expectation that IIR filters are far more computationally efficient for equivalent frequency selectivity.

5.3 Frequency Response Verification

The frequency responses of all three filter implementations were verified by sweeping a sinusoidal input from 10 Hz to 990 Hz and measuring the output amplitude. All filters demonstrated responses within ± 0.5 dB of their theoretically designed responses across the passband, confirming correct coefficient computation and implementation. The IIR Butterworth filter achieved a stopband attenuation of 50.2 dB (theoretical: 51.1 dB), with the 0.9 dB discrepancy attributable to single-precision floating-point rounding in the biquad coefficient representation.

5.4 ECG Signal Denoising Performance

Table 3 shows SNR improvement results for ECG signal processing. The input signal was a clean ECG corrupted with three types of noise: 50 Hz power-line interference (PLI), baseline wander (0.05-0.5 Hz), and broadband white Gaussian noise.

Table 3. ECG signal-to-noise ratio improvement (dB).

Noise Type	Input SNR (dB)	FIR Output (dB)	IIR Output (dB)	LMS Output (dB)
50 Hz PLI	12.3	31.5	28.9	40.2
Baseline Wander	15.7	38.1	41.6	N/A



White Gaussian	10.2	24.7	22.3	19.8
Combined	8.9	26.3	27.1	32.4

The LMS adaptive filter dramatically outperforms both FIR and IIR filters for narrowband 50 Hz interference removal, achieving 40.2 dB SNR improvement versus 31.5 dB (FIR) and 28.9 dB (IIR). This is because the LMS filter continuously adapts to the exact phase and amplitude of the interference, achieving near-perfect cancellation. For broadband noise, however, the fixed FIR filter performs best, as the LMS filter's adaptation can be confused by high noise power.

5.5 Power Consumption

Table 4 shows power consumption measured at 3.3 V supply with the filter running continuously at 1 kHz.

Table 4. System power consumption.

Configuration	Supply Current (mA)	Power (mW)	vs. Baseline (%)
Baseline (CPU idle, peripherals off)	14.2	46.9	0%
ADC + DMA only (no filter)	16.8	55.4	+18%
FIR Order-64 (optimized)	18.1	59.7	+27%
IIR 8th-order Butterworth	17.5	57.8	+23%
LMS Order-32 ($\mu=0.005$)	17.9	59.1	+26%
Full system (IIR + ADC + DAC + DMA)	19.3	63.7	+36%

The full system including ADC acquisition, IIR filtering, and DAC output via DMA consumes only 63.7 mW, with the filter computation itself adding only 2.4 mW above the ADC+DMA baseline. This demonstrates that the DMA architecture successfully offloads data movement from the CPU, keeping filter-related power overhead minimal. The IIR filter consumes the least power due to its lower cycle count, making it the preferred choice for battery-powered applications.

5.6 Audio and Industrial Vibration Results

For audio signal processing, the FIR and IIR filters were applied to remove 60 Hz electrical hum from microphone recordings. The IIR notch filter (2nd-order, $Q=30$) achieved 52 dB rejection of the 60 Hz tone with negligible audible effect on surrounding frequencies, completing in just 18 cycles per sample.

For industrial vibration monitoring, an accelerometer signal (ADXL345, SPI interface, 800 Hz) was processed with a bandpass IIR filter (20-500 Hz, 4th-order Butterworth) to isolate bearing fault frequencies. The system successfully detected a characteristic defect frequency at 87 Hz in the filtered spectrum that was completely masked by low-frequency vibration in the raw signal, demonstrating the practical utility of the implemented system.

6. Discussion

6.1 Filter Selection Guidelines

Based on our experimental results, we propose the following guidelines for filter selection in embedded DSP applications. These are not rigid rules but engineering trade-offs that must be evaluated against application requirements.



FIR filters are the best choice when linear phase response is required (such as in communications systems where phase distortion causes inter-symbol interference), when the filter needs to be easily redesigned at runtime (since only coefficient update is needed, with no stability concerns), or when the application requires exact zero-phase filtering on recorded data (using offline processing).

IIR filters are the best choice for most real-time filtering applications that do not require linear phase, particularly when computational efficiency is paramount. An 8th-order Butterworth IIR filter achieves 50 dB stopband attenuation using 4.7x fewer operations than an equivalent FIR filter, directly translating to longer battery life in portable devices.

Adaptive LMS filters are the best choice when the noise to be removed is narrowband, correlated, and has a reference signal available — the classic example being 50/60 Hz power-line interference in biomedical signals. In this application, the LMS filter outperforms both FIR and IIR by a wide margin, achieving 28 dB better SNR improvement for PLI removal.

6.2 Hardware-Software Co-Design Insights

The most important lesson from this work is that embedded DSP performance is not determined by algorithm choice alone — hardware resource utilization is equally important. Three specific co-design decisions had major impact on system performance. First, enabling the FPU reduced FIR filter computation time by 38% compared to software floating-point emulation. Engineers should always explicitly enable the FPU in Cortex-M4 startup code, as it is disabled by default. Second, using DMA for ADC data transfer reduced the CPU's data movement overhead from 22% to less than 1% of total cycles, freeing the processor almost entirely for filter computation. Third, the double-buffering architecture eliminated the need for critical section protection of the sample buffer, avoiding priority inversion problems that can cause timing jitter in interrupt-driven systems.

6.3 Limitations and Future Work

This work has several limitations that suggest directions for future research. The current implementation processes signals from a single channel; multi-channel applications (such as a 12-lead ECG or a microphone array) would require parallel filter instances and more sophisticated DMA scheduling. The LMS step size μ is currently fixed; a variable step-size LMS (VSSLMS) or recursive least squares (RLS) algorithm would achieve faster convergence without sacrificing steady-state performance. Finally, the current implementation uses 32-bit single-precision floating point throughout; future work should investigate fixed-point (Q15 or Q31) implementations, which can achieve 2-4x throughput improvement on the Cortex-M4 DSP extension instructions, potentially enabling much higher sampling rates or larger filter orders within the same power budget.

7. Conclusion

This paper has presented a complete hardware-software co-design approach to real-time digital signal filtering on embedded systems, spanning from mathematical filter theory through circuit design to optimized firmware implementation and empirical performance evaluation.

We implemented three filtering architectures — FIR, IIR (cascaded biquads), and adaptive LMS — on an ARM Cortex-M4 microcontroller at 168 MHz. By strategically using hardware resources including the FPU, DMA controller, and double-buffering, we achieved highly efficient real-time operation: the



optimized IIR filter processes one sample in 87 clock cycles (0.52 μ s), leaving 95% of CPU capacity available, while consuming only 57.8 mW total system power.

The LMS adaptive filter demonstrated remarkable performance for biomedical ECG denoising, achieving 40.2 dB SNR improvement for 50 Hz power-line interference removal — 8.7 dB better than the best fixed filter. For applications requiring low computational cost with good general-purpose frequency selectivity, the IIR Butterworth filter is the clear winner, requiring 4.7x fewer operations than an equivalent FIR design.

The central contribution of this paper is not any individual result but the integrated perspective: a single embedded system can be understood from the differential equation describing the filter, to the silicon transistors executing the computation, to the milliwatts consumed by the battery. Engineers who understand both the hardware and the software of their systems can extract performance that neither a pure software engineer nor a pure hardware engineer could achieve alone. This hardware-software co-design mindset is the foundation of modern embedded electronic engineering.

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